REMARKS

Claims 1-26 are pending in the present application. Claims 1, 4, 8, 16, 20 and 23-26 have been amended. No new matter has been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

Applicant thanks the Examiner for discussing this case with Applicant on August 4, 2009. The Examiner's comments and suggestions have been incorporated herein.

Claims 1, 3-13 and 16-26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrell, *et al.* (U.S. Patent No. 5,829,038, hereinafter "Merrell") and further in view of "The Cache Memory Book" by Jim Handy (hereinafter, "Handy"), claim 2 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrell, in view of Handy as applied to claim 1, and further in view of Klein (U.S. Patent No. 6,401,199 B1, hereinafter "Klein"), claims 14 and 15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrell, in view of Handy as applied to claim 13, and further in view of Stewart, *et al.* (U.S. Patent No. 5,157,780, hereinafter "Stewart"). Applicant respectfully traverses these rejections.

In response to a discussion with the Examiner during the telephone interview, claim 1 has been amended to recite, "discard all the cache mirror data designated to be written to an external memory received from the processor chip so that any of the data written to the internal data cache is never written to any external memory during operation of the processor chip." The Office Action associates Merrell's writeback process with writing to external memory. (Office Action, page 4.) Merrell teaches writing the cache memory at least some of the time. (Merrell, Figure 3; col. 4, lines 46-50.) Applicant further notes that Merrell is directed toward a cache structure for a single processor. (Merrell, Figure 3; col. 2, lines 54-65.) In fact, the writing of the memory "is cancelled only if an associated cache line is found already having a 'modified' status in a lower

level cache." (Merrell, col. 4, lines 46-50; emphasis added.) Merrell, therefore, teaches away from the amended limitation of "any of the data written to the internal data cache is never written to any external memory." Furthermore, Handy does not teach this limitation. Applicant, therefore, respectfully submits that claim 1 is patentable over the prior art of record.

Claims 2, 3, 5-7, 19 and 20 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claim 4 has been amended to recite, "any data written to the internal data cache is never written to any external memory during operation of the processing chip." As is discussed hereinabove with respect to claim 1, Merrell teaches writing the cache memory at least some of the time. (Merrell, Figure 3; col. 4, lines 46-50.) Merrell, therefore, teaches away from the limitation of "any data written to the internal data cache is never written to any external memory during operation of the processing chip." Furthermore, Handy does not teach or suggest this limitation. Applicant, therefore, respectfully submits that claim 4 is patentable over the prior art of record.

Claims 21 and 22 depend from claim 4 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claim 8 has been amended to recite, "any of the data written to the internal data cache is never written to any external memory." As is discussed hereinabove with respect to claim 1, Merrell teaches writing the cache memory at least some of the time. (Merrell, Figure 3; col. 4, lines 46-50.) Merrell, therefore, teaches away from the limitation of "any of the data written to the internal data cache is never written to any external memory." Furthermore, Handy does not

teach or suggest this limitation. Applicant, therefore, respectfully submits that claim 8 is patentable over the prior art of record.

Claims 9-15, 23 and 24 depend from claim 8 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claim 16 has been amended to recite, "any of the data written to the internal data cache of the first integrated circuit is never written to any external memory during operation of a first processor on the first integrated circuit." As is discussed hereinabove with respect to claim 1, Merrell teaches writing cache memory at least some of the time. (Merrell, Figure 3; col. 4, lines 46-50.) Applicant further notes that Merrell is directed toward a cache structure for a single processor. (Merrell, Figure 3; col. 2, lines 54-65.) Merrell, therefore, teaches away from the limitation of "any of the data written to the internal data cache of the first integrated circuit is never written to any external memory during operation of a first processor on the first integrated circuit." Furthermore, Handy does not teach or suggest this limitation. Applicant, therefore, respectfully submits that claim 16 is patentable over the prior art of record.

Claims 17, 18, 25 and 26 depend from claim 16 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Benjamin E. Nise, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge, or credit any overpayment, Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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